REMARKS

Reconsideration of the present application is respectfully requested. Claims 2-5, 7-11, 18-21 and 31-38 previously presented for examination remain in the application. Claims 3, 4, 7, 8, 10, 11, 31, 32, and 34-37 have been amended, not for prior art reasons, but to more particularly point out and distinctly claim the subject matter that applicants regard as the invention. No claims have been canceled or added.

Claims 31-33 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4, 31-32 and 34-35 stand objected to for minor informalities. Applicants have corrected the informalities as indicated in the claim amendments herein. In particular, applicants have clarified in claim 4 that the frequency multiplying circuit is to receive the distributed clock signal and provide an output clock signal the duty cycle correction circuit as indicated. Applicants respectfully submit that the claims are in proper form.

Claims 7-11 and 37-38 stand rejected under 35 U.S.C. § 112, second paragraph as being considered to be indefinite. In particular, it is stated that the recitation in claim 37 that the duty cycle correction circuit is to generate a reference voltage signal is misdescriptive. Applicants respectfully submit that this is not the case and support for such a claim is clearly provided in the specification and figures as filed. (See, for example, Figure 2 (where duty cycle correction circuit generates pref and nref signals and Figure 7 where pref and

nref signals are used to control clock generation circuit 710, and accompanying description beginning at page 25, line 15.)

Applicants have amended the claims as indicated to more particularly point out and distinctly claim the subject matter that Applicants regard as the invention. Applicants respectfully submit that the claims meet the requirements of 35 U.S.C. § 112.

Claims 2-5, 7-11, 18-21, 34-35 and 37-38 stand rejected under 35 U.S.C. § 102(b) as being considered unpatentable over U.S. Patent No. 5,122,679 to Ishii et al. ("Ishii").

Applicants respectfully submit that Ishii fails to teach or suggest at least the duty cycle correction circuit as set forth in claim 4.

Claim 4 includes the limitations

> a clock distribution network to distribute a clock signal on an integrated circuit chip;
> a duty cycle correction circuit at a receiver in the clock distribution network; and
> frequency multiplying circuitry coupled to the duty cycle correction circuit, the frequency multiplying circuitry to receive a distributed clock signal received at the receiver at an input and provide an output clock signal having a frequency that is a multiple of the distributed clock signal,
> the duty cycle correction circuit to correct a duty cycle of the output clock signal and provide a duty-cycle-corrected output clock signal.

(Claim 4)(emphasis added).

Ishii discloses an integrated logic circuit with clock skew adjusters. In accordance with Ishii, clock skew adjustors include variable clock delay means, phase comparator means and a frequency divider and the wiring distances between once clock source and the individual clock skew adjustors are

substantially equalized. The variable delay means of the Ishii is controlled by feeding a common frequency information and a phase information signal to the individual clock skew adjustors from one clock source to feed the adjusted clock to a flip-flop and by feeding back the clock from the clock input terminal of a destination circuit to the phase comparator of the clock skew adjustor to detect the phase difference from the phase information signal so that the phase difference may be reduced to zero. (Ishii, col. 1, lines 52 - 66).

Using the means described above, according to Ishii, it is possible to prevent the signal transmission delay difference between the clock source and the individual clock skew adjustors. (Ishii, col. 1, line 67 - col. 2, line 2).

As is well-known in the art, clock skew is defined as the difference in arrival times of a clock signal at different destinations. In other words, clock skew is the signal transmission delay difference between a clock source and at least two different destinations. Therefore, Ishii is directed to adjusting for signal transmission delay differences by varying the delay applied to different signals.

In contrast, claim 4 sets forth a duty cycle correction circuit. As is well-known in the art, the term duty cycle refers to the ratio of pulse duration or pulse width to the overall cycle time of a signal. For an exemplary signal, for example, the term duty cycle may refer to the ratio of the time the signal is high to the overall cycle time of the signal. Thus, a duty cycle correction circuit as set forth in claim 4 operates, not to adjust clock skew as disclosed in Ishii, but to correct the duty cycle of a signal.

Ishii does not teach or suggest correcting at a duty cycle of a signal. For at least this reason, claim 4 is patentably distinguished over Ishii.

Each of independent claims 8 and 18 also set forth a similar limitation as argued above in reference to claim 4. Claims 2-3, 5, and 31-38, claims 7 and 9-11 and claims 19-21 depend from and further limit claims 4, 8 and 18, respectively. Thus, claims 2-3, 5, 7-11, 18-21 and 31-38 are also patentably distinguished over the Ishii reference for at least the same reason.

Based on the foregoing, applicants respectfully submit that the applicable rejections and objections have been overcome and claims 2-5, 7-11, 18-21, and 31-38 are in condition for allowance. If the examiner disagrees or believes that further discussion will expedite prosecution of this case, the examiner is invited to telephone applicants' representative at the number indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: 6/20, 2003

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